

FIG. 1

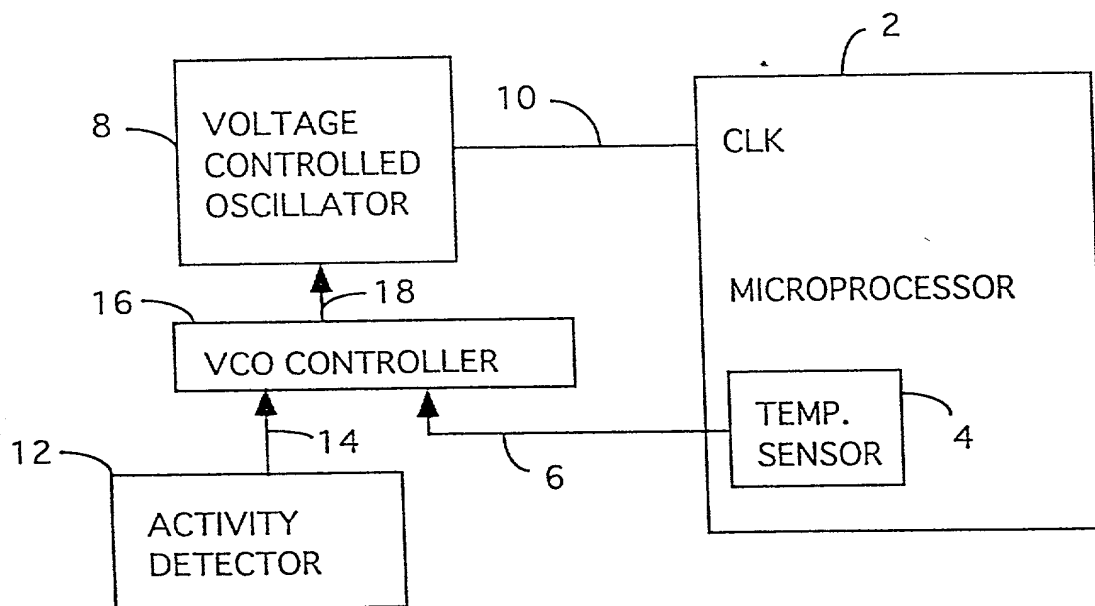


FIG. 3

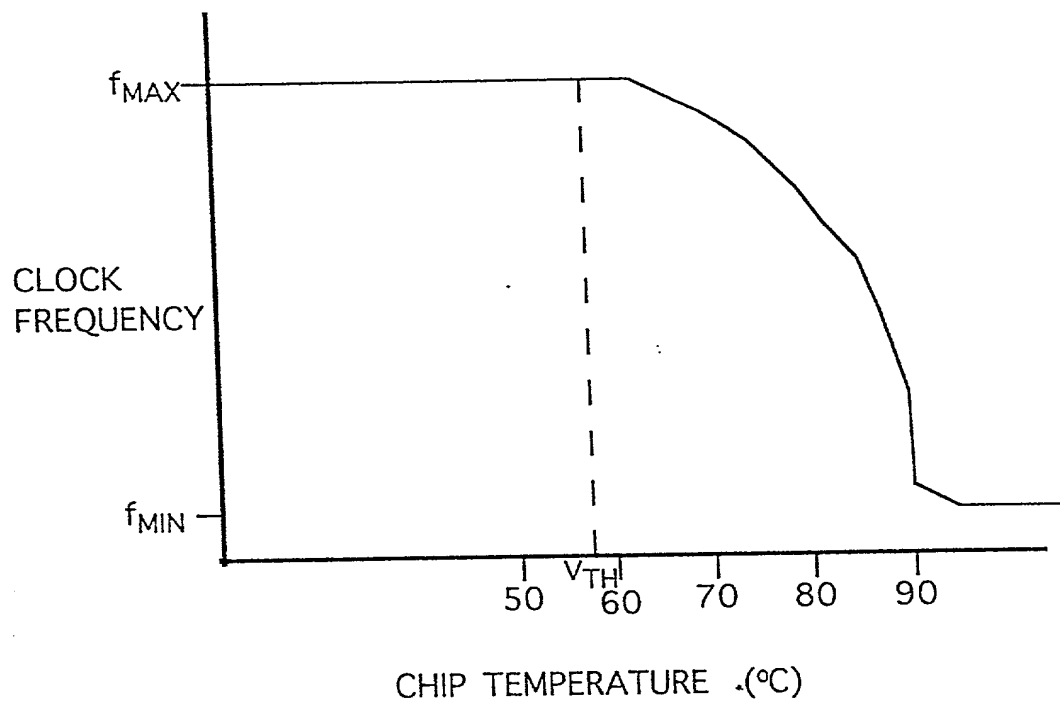


FIG. 2

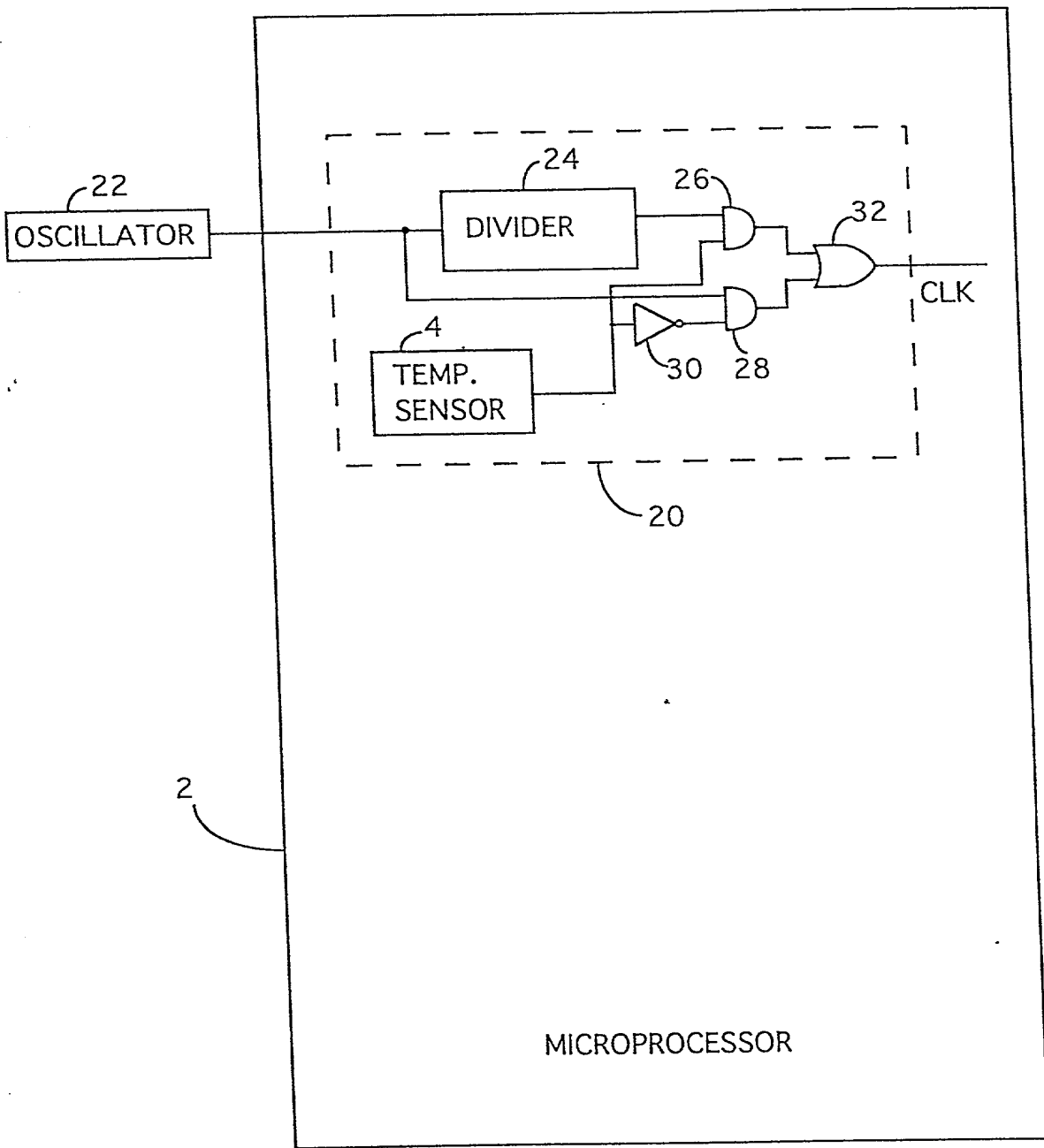


FIG. 4

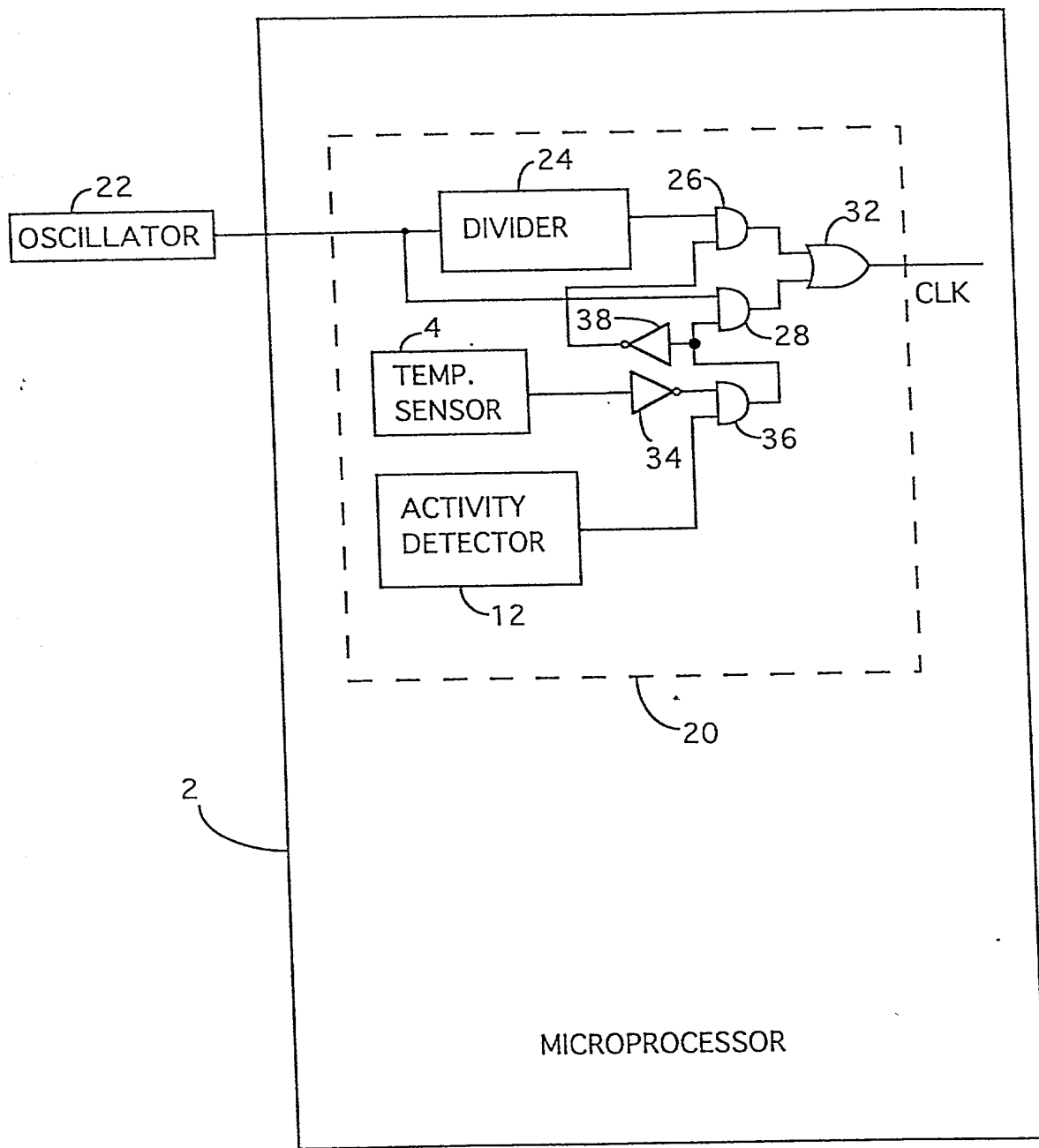


FIG. 5

FIG. 6 is a timing diagram showing the relationship between the FAST CLK, SLEEP CLK, TEMP SIGNAL, ACTIVITY SIGNAL, and OUTPUT CLOCK (CLK) signals.

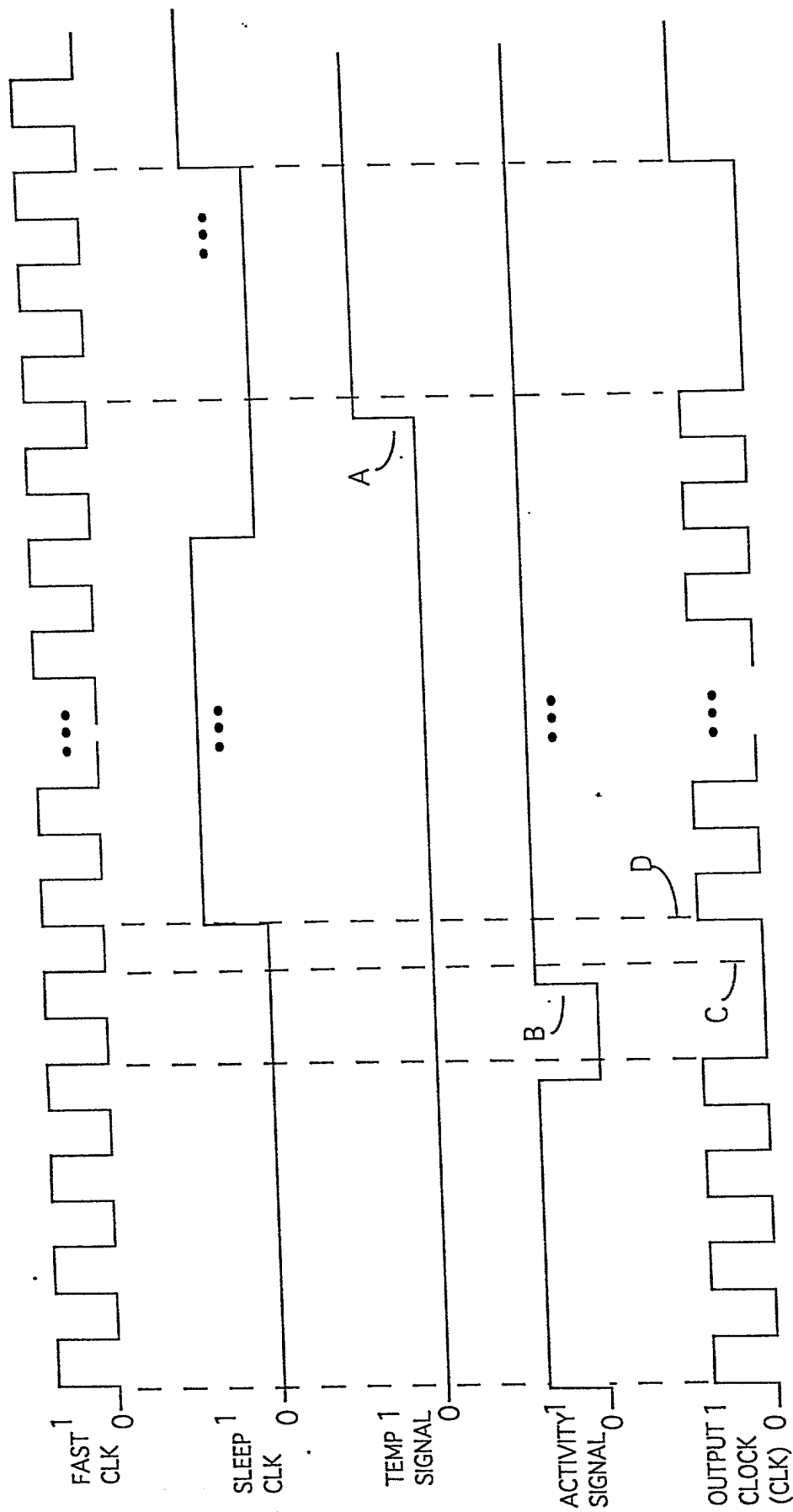


FIG. 6

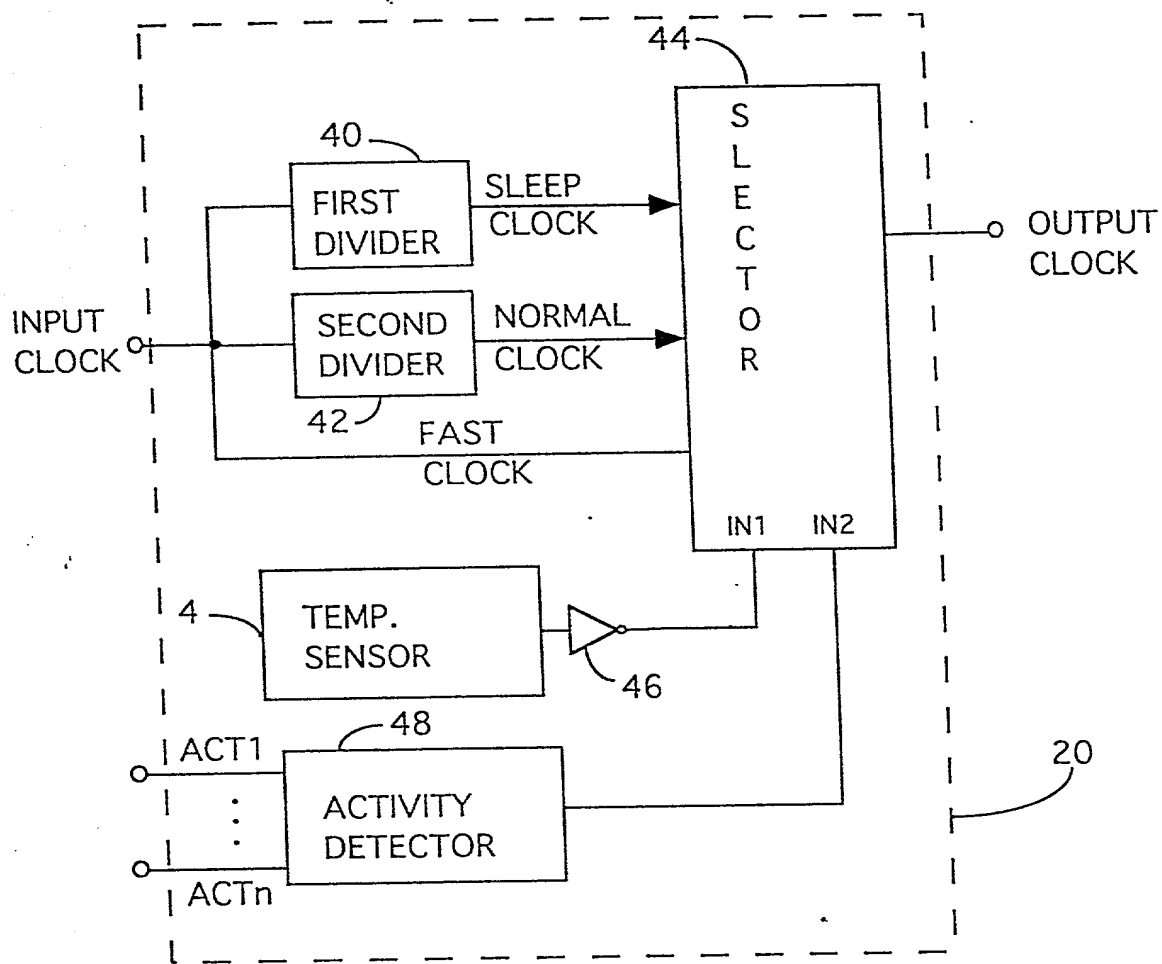


FIG. 7

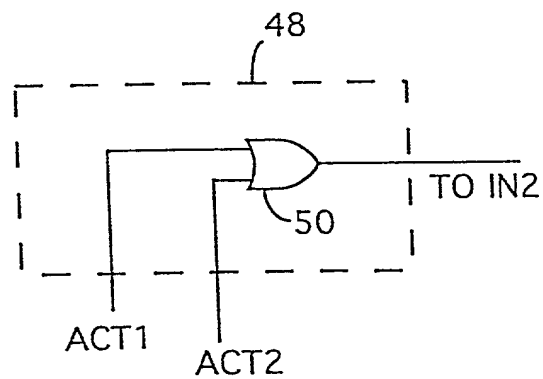


FIG. 8

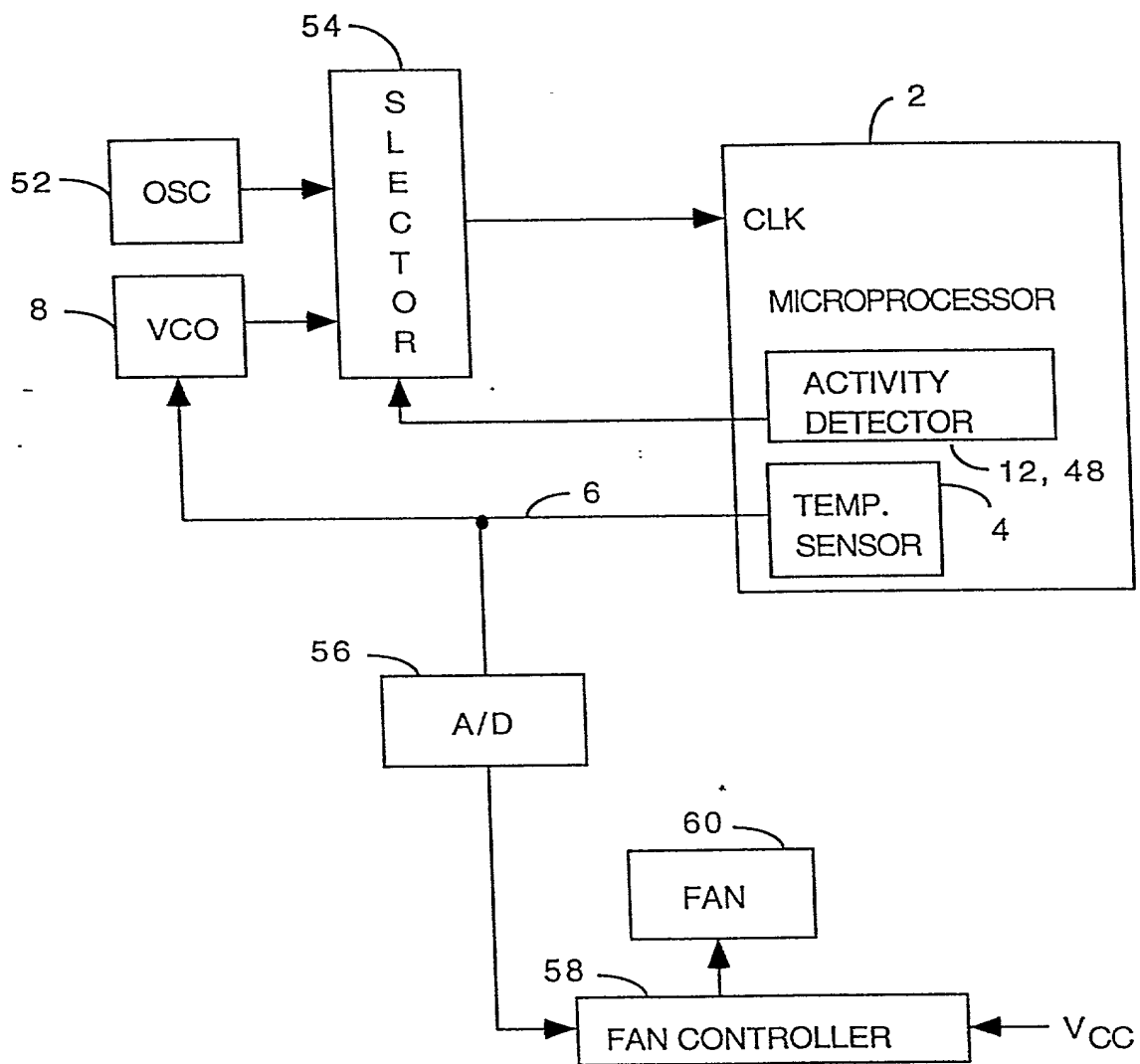


FIG. 9

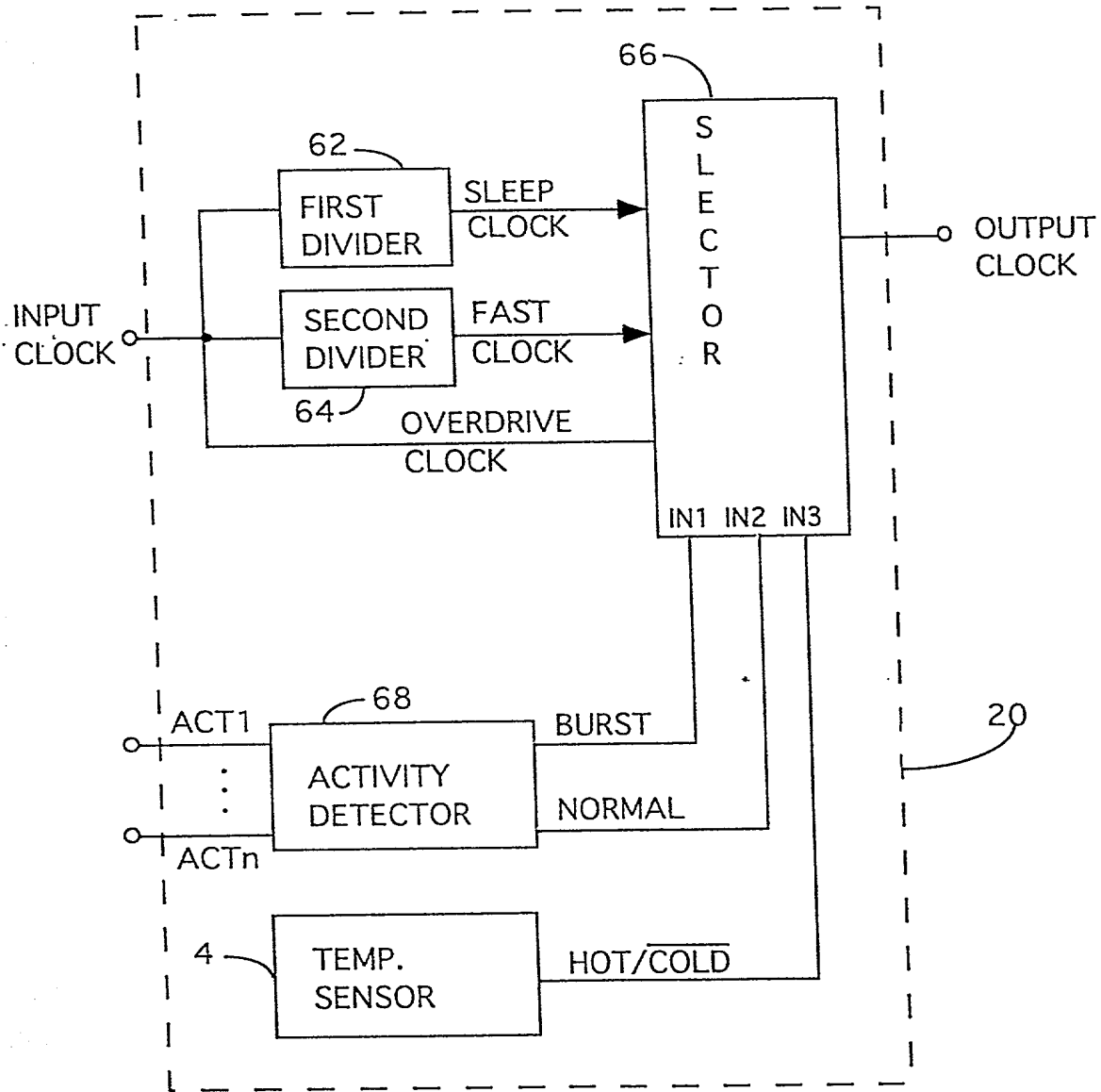


FIG. 10